Chapter 5

FIELD-EFFECT TRANSISTORS (FETs)

FETs is also a three terminal devices. For the FET an electric field is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

Differences

BJTs | FETs
---|---
(i) Current-controlled devices | (i) Voltage-controlled devices

Current $I_C$ is a direct function of the level of $I_B$.

(ii) Bipolar device (n-p-n and p-n-p)
Conduction level is a function of Two carriers, electrons and holes.

Current $I_D$ is a function of the voltage $V_{GS}$ applied to the input circuit.

(ii) Unipolar device (n-channel and p-channel)
Conduction level is a function of one type of carrier, either electrons (n-channel) or holes (p-channel).
Types of FETs:
(i) Junction FETs (JFET) and
(ii) Metal-Oxide-Semiconductor FETs (MOSFET)

MOSFET can be divided to two types:
(i) Depletion type and
(ii) Enhancement type.

The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design.

CONSTRUCTION and CHARACTERISTICS of JFETs

Ex: n-channel JFETs

The major part of the structure is the n-type material that forms the channel between the embedded layers of p-type material.

The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain (D), while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S).

The two p-type materials are connected together and to the gate (G) terminal. Therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material.

Under no-bias condition, there are two p-n junctions. The result is a depletion region at each junction. A depletion region is that region void of free carriers and therefore unable to support conduction through the region.
The source of water pressure can be likened to the applied voltage from drain to source that will establish a flow of water (electrons) from the spigot (source). The "gate", through an applied signal (potential), controls the flow of water (charge) to the "drain". The drain and source terminals are at opposite ends of the n-channel because the terminology is defined for electron flow.

$V_{GS} = 0\text{V}, V_{DS} \text{ Some Positive Value}$

In this figure, a positive voltage $V_{DS}$ has been applied across the channel and the gate has been connected directly to the source to establish the condition $V_{GS}=0\text{V}$.

The result is a gate and source terminal at the same potential and a depletion region in the low end of each p-material similar to the distribution of the no-bias condition.

The instant the voltage $V_{DD} (=V_{DS})$ is applied the electrons will be drawn to the drain terminal, establishing the conventional current $I_D$. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D=I_S$).

The flow of charge is limited solely by the resistance of the n-channel between drain and source.
It is noted here that the depletion region is wider near the top of both p-type materials. Assuming a uniform resistance in the n-channel, the resistance of the channel can be broken down to the divisions shown in the figure. The current $I_D$ will establish the voltage levels through the channel as indicated on the same figure.

For example, the upper region of the p-type material will be reverse-biased by about 1.5V, with the lower region only reverse-biased by 0.5V.

Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider the depletion region.

The fact that the p-n junction is reverse biased for the length of the channel results in a gate current of zero amperes. The fact that $I_G=0$A is an important characteristics of the JFET.

As the voltage $V_{DS}$ is increased from 0 to a few volts, the current will increase as determined by Ohm's law. The relative straightness of the plot reveals that for the region of low values of $V_{DS}$, the resistance is essentially constant.

As $V_{DS}$ increases and approaches a level referred to as $V_P$, the depletion region will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph to occur. The more horizontal the curve, the higher the resistance. If $V_{DS}$ is increased to a level where it appears that the two depletion regions would "touch" as shown in the figure, the condition is referred to as "Pinch Off" will result.
In the saturation region, the level of $I_D$ remains essentially the same. Therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a source current. As shown in the previous figure (output characteristics), the current is fixed at $I_D = I_{DSS}$ but the voltage $V_{DS}$ (for levels $> V_P$) is determined by the applied load.

The notation of $I_{DSS}$ is derived from the fact that it is the Drain-to-Source current with a Short-circuit connection from gate to source.

$I_{DSS}$ is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0V$ and $V_{GS} > V_P$.

$V_{GS} < 0V$

$V_{GS}$ is the voltage from gate to source and is the controlling voltage of the JFET.

For the n-channel device the controlling voltage $V_{GS}$ is made more and more negative from its $V_{GS} = 0V$ level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

In the figure, a negative voltage of $-1V$ has been applied between the gate and source terminals for a low level of $V_{DS}$. The effect of the applied negative-bias $V_{GS}$ is to establish depletion regions similar to those obtained with $V_{GS} = 0V$ but at lower levels of $V_{GS}$. The result of applying a negative bias to the gate is to reach the saturation level at a lower level of $V_{DS}$. The resulting saturation level for $I_D$ has been reduced and in fact will continue to decrease as $V_{GS}$ is made more and more negative.
The pinch-off voltage continues to drop in a parabolic manner as $V_{GS}$ becomes more and more negative. Eventually, $V_{GS}$ when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, for all practical purposes the device has been "turned off".

![Graph showing the loci of pinch-off values and ohmic region]

The level of $V_{GS}$ that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$ with $V_P$ being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

Chapter 5  FETs

Voltage-Controlled Resistor

The region to the left of the pinch-off locus is referred to as ohmic or voltage-controlled resistance region. In this region, the JFET can actually be employed as a variable resistor whose resistance is controlled by the applied gate-to-source voltage.

Note that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} < V_P$ is a function of the applied voltage $V_{GS}$. As $V_{GS}$ becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding with an increasing resistance level.

The following equation will provide a good approximation to the resistance level in terms of the applied voltage $V_{GS}$.

\[ r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^3} \]

Where $r_o$ is the resistance with $V_{GS} = 0$V and $r_d$ the resistance at a particular level of $V_{GS}$. For an n-channel JFET with $r_o$ equal to 10 kOhm ($V_{GS} = 0$V, $V_P = -6$V), the above equation will result in 40 kOhm at $V_{GS} = -3$V.
p-Channel Devices

The p-channel JFET is constructed in exactly the same manner as the n-channel device. The defined current directions are reversed as are the actual polarities for the voltage $V_{GS}$ and $V_{DS}$.

For the p-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for $V_{DS}$ will result in negative voltages for $V_{DS}$ on the above output characteristics which has an $I_{DS}$ of 6 mA and a pinch-off voltage of $V_{GS} = +6V$. The minus signs for $V_{DS}$ simply indicate that the source is at a higher potential than the drain.

Symbols

The arrow is pointing in for n-channel device to represent the direction in which $I_G$ would flow if the p-n junction were forward-biased. The only difference in the symbol is the direction of the arrow.
SUMMARY
(i) The maximum current is defined as $I_{DSS}$ and occurs when $V_{GS} = 0\,V$ and $V_{DS} \geq |V_p|$
(ii) For gate-to-source voltages $V_{GS}$ less than (more negative than) the pinch-off level, the drain current is 0A ($I_D = 0A$).
(iii) For all levels of $V_{GS}$ between 0V and the pinch-off level, the current $I_D$ will range between $I_{DSS}$ and 0A, respectively.
(iv) For p-channel JFETs a similar list mentioned above can be developed.

TRANSFER CHARACTERISTICS
For the BJTs, the output current $I_C$ and input controlling current $I_B$ were related by beta.

$$I_C = f(I_B) = \beta I_B$$

A linear relationship exists between $I_C$ and $I_B$. Double the level of $I_B$ and $I_C$ will increase by a factor of two also.

The above linear relationship does not exist between the output and input quantities of a JFET. The relationship between $I_D$ and $V_{GS}$ is defined by Shockley’s equation.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_T}\right)^2$$

The squared term of the equation will result in a nonlinear relationship between $I_D$ and $V_{GS}$, producing a curve that grows exponentially with decreasing magnitudes of $V_{GS}$.

DC analysis can be performed using a graphical approach and mathematical approach. Graphical approach is more direct and easier to apply. However, it require a plot of above equation to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves.
The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

Obtaining transfer curve: When \( V_{GS} = 0 \) V, \( I_D = I_{DSS} \)
When \( V_{GS} = V_P \), \( I_D = 0 \) mA

The transfer characteristics are a plot of an output current versus an input-controlling quantity. Therefore, there is a direct "transfer" from input to output variables.

If the relationship were linear, the plot of \( I_D \) versus \( V_{GS} \) would result in a straight line between \( I_{DSS} \) and \( V_P \). However, a parabolic curve will result because the vertical spacing between steps of \( V_{GS} \) on the drain characteristics decreases noticeably as \( V_{GS} \) becomes more and more negative.

Compare the spacing between \( V_{GS} = 0 \) V and \( V_{GS} = -1 \) V to that between \( V_{GS} = -3 \) V and pinch-off. The change in \( V_{GS} \) is the same but the resulting change in \( I_D \) is quite different.

* A quick, efficient method of plotting \( I_D \) versus \( V_{GS} \) given only the levels of \( I_{DSS} \) and \( V_P \) and Shockley's equation.

Applying Shockley’s Equation

Examining a few specific levels.

(i) \( V_{GS} = 0 \) V

\[
I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2
= I_{DSS} \left( 1 - \frac{0}{V_P} \right)^2 = I_{DSS}(1 - 0)^2
\]
(ii) $V_{GS} = V_F$

\[
I_D = I_{DSS} \left( 1 - \frac{V_F}{V_P} \right)^2 = I_{DSS} (1 - 1)^2 = I_{DSS} (0)
\]

$I_D = 0 \text{ A} |_{V_{GS} = V_F}$

(iii) Selected curve; ex. $V_{GS} = -1 \text{ V}$

\[
I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2
= 8 \text{ mA} \left( 1 - \frac{-1 \text{ V}}{-4 \text{ V}} \right)^2
= 8 \text{ mA} \left( 1 - \frac{1}{4} \right)^2
= 8 \text{ mA}(0.75)^2
= 4.5 \text{ mA}
\]

Note the care taken with the negative signs for $V_{GS}$ and $V_F$ in the calculations above. The loss of one sign would result in a totally erroneous result.

It should be obvious from the above that the level of $I_D$ can be found for any level of $V_{GS}$.

Using basic algebra, we can obtain an equation for the resulting level of $V_{GS}$ for a given level of $I_D$.

\[
V_{GS} = V_F \left( 1 - \frac{I_D}{I_{DSS}} \right)
\]

We can test the above equation using the previous output characteristics.

\[
V_{GS} = -4 \text{ V} \left( 1 - \frac{4.5 \text{ mA}}{8 \text{ mA}} \right)
= -4 \text{ V}(1 - \sqrt{0.5625})
= -4 \text{ V}(0.75)
= -1 \text{ V}
\]
Shorthand Method

Since the transfer curve must be plotted so frequently, it would be quite advantageous to have a shorthand method for plotting the curve in the quickest, most efficient manner while maintaining an acceptable degree of accuracy.

(i) If we specify $V_{GS}$ to be one-half the pinch-off value $V_P$, the resulting level of $I_D$ will be the following, as determined by Shockley's equation:

\[
I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2
\]

\[
= I_{DSS} \left(1 - \frac{V_P/2}{V_P}\right)^2 = I_{DSS} \left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.25)^2
\]

\[
I_D = \frac{I_{DSS}}{4} \mid V_{GS} = V_P / 2
\]

The result specifies that the drain current will always be one-fourth of the saturation level $I_{DSS}$ as long as the gate-to-source voltage is one-half the pinch-off value.

(ii) If we choose $I_D = I_{DSS}/2$, we find that

\[
V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)
\]

\[
= V_P \left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)
\]

\[
V_{GS} = 0.3V_P \mid I_D = I_{DSS}/2
\]

As conclusion, the transfer curve can be sketched to a satisfactory level of accuracy simply using the four plot points.
**Example (1):** Sketch the transfer curve defined by $I_{DSS} = 12 \text{ mA}$ and $V_P = -6\text{ V}$.

**Solution:**

Four points;

(i) $I_{DSS} = 12 \text{ mA}$ and $V_{GS} = 0 \text{ V}$

(ii) $I_D = 0 \text{ mA}$ and $V_{GS} = V_P$

(iii) $V_{GS} = V_P/2 = -6 \text{ V}/2 = -3 \text{ V}$

$$I_{DSS}/4 = 12 \text{ mA}/4 = 3 \text{ mA}$$

(iv) $I_D = I_{DSS}/2 = 12 \text{ mA}/2 = 6 \text{ mA}$

$$V_{GS} = 0.3V_P = 0.3(-6 \text{ V}) = -1.8 \text{ V}$$

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**Example (2):** Sketch the transfer curve for a p-channel defined by $I_{DSS} = 4 \text{ mA}$ and $V_P = 3\text{ V}$.

**Solution:**

$$V_{GS} = V_P/2 = 3 \text{ V}/2 = 1.5 \text{ V}$$

$$I_D = I_{DSS}/4 = 4 \text{ mA}/4 = 1 \text{ mA}$$

$$I_D = I_{DSS}/2 = 4 \text{ mA}/2 = 2 \text{ mA}$$

$$V_{GS} = 0.3V_P = 0.3(3 \text{ V}) = 0.9 \text{ V}$$
For the BJT configuration, $I_B$ is normally the first parameter to be determined.
For the JFET, it is normally $V_{GS}$.

**DEPLETION-TYPE MOSFET**

**Basic Construction**

A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation upon which the device will be constructed.

In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device.

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide ($\text{SiO}_2$) layer.

$\text{SiO}_2$ is an insulator. Therefore, there is no direct electrical connection between the gate terminal and the channel of a MOSFET.
SiO₂ is a insulator: (ii) Therefore, it construct very high input impedance of the device. Then it support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configuration.

Metal-Oxide-Semiconductor FET or another name Insulated-Gate FET (IGFET)

Metal: for the drain, source and gate connections to the proper surface- in particular the gate terminal and the control to be offered by the surface area of the contact.

Oxide: Silicon dioxide insulating layer.

Semiconductor: the basic structure on which the n- and p-type regions are diffused.

Basic Operation and Characteristics

The gate-to-source voltage VGS is set to zero volts by the direct connection from one terminal to the other and a voltage VDS is applied across the drain-to-source terminals.

The results is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with $V_{GS} = 0\,\text{V}$ continues to be labeled $I_{DSS}$. 
Let set \( V_{GS} \) to a negative voltage such as \(-1\) V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charge attract).

Depending on the magnitude of the negative bias established by \( V_{GS} \), a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction.

The more negative the bias, the higher rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for \( V_{GS} \).
For positive values of $V_{GS}$, the positive gate will draw additional electrons (free carriers) from the p-type substrate and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage, $V_{GS}$ continues to increase in the positive direction reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS} = 0V$ and $V_{GS} = +1V$ curves is a clear indication of how much the current has increased for the 1 V change in $V_{GS}$. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} =0V$. For this reason, the region of positive gate voltages on the drain or transfer characteristics is often referred to as the "enhancement region", with the region between cut-off and the saturation level of $I_{DSS}$ referred to as the "depletion region".

Example (3): Sketch the transfer characteristics for an n-channel depletion type MOSFET with $I_{DSS} = 10 mA$ and $V_P = -4 V$.

Solution:

Before plotting the positive region of $V_{GS}$, keep in mind that $I_D$ increases very rapidly with increasing positive values of $V_{GS}$. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we will try +1V as follows:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10 mA \left(1 - \frac{-1 V}{4 V}\right)^2 = 10 mA (1 + 0.25)^2 = 10 mA (1.5625)$$

$$= 15.63 mA$$
p-Channel Depletion Type MOSFET

The construction of a p-channel depletion type MOSFET is exactly the reverse of that n-channel depletion type MOSFET. There is now an n-type substrate and a p-type channel. The terminals remain as identified but all the voltage polarities and the current directions are reversed. $V_{DS}$ will have negative values and $I_D$ will have positive values since the defined direction is now reversed. The reversal in $V_{GS}$ will result in a mirror image for the transfer characteristics.

Symbols

The symbols chosen try to reflect the actual construction of the device. The lack of a direct connection (due to the gate insulation) between the gate and channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and source and is “supported” by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available while in others it is not. For most of the analysis, the substrate and source will be connected and lower symbols will be employed.
Although there are some similarities in construction and mode of operation between depletion-type and enhancement type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley’s equation and the drain current is now cut off until the gate-to-source voltage $V_{GS}$ reaches a specific magnitude.

Basic Construction of n-channel Enhancement type MOSFET

A slab of p-type material is formed from a silicon base and is again referred to as substrate.

Note here the absence of a channel between the two n-doped regions. This is the primary difference between the construction of depletion type and enhancement type MOSFETs.

Basic Operation and Characteristics

(i) $V_{GS} = 0$ V and a voltage applied between the drain and source of the device, $V_{DS}$ will result in a current of effectively zero amperes.

With $V_{DS}$ some positive voltage, $V_{GS} = 0$ V and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between the drain and source.

(ii) Both $V_{DS}$ and $V_{GS}$ have been set at some positive voltage greater than 0V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes in the p-substrate along the edge of the SiO₂ layer to leave the area and enter deeper regions of the p-substrate. The result is a depletion region near the SiO₂ insulating layer void of holes.
However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO₂ layer. The SiO₂ layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V₆GS increases in magnitude, the concentration of electrons near the SiO₂ surface increases until eventually the induced n-type region can support a measurable flow between drain and source.

The level of V₆GS that results in the significant increase in drain current is called the threshold voltage, V₆T. On specification sheets it is referred to as V₆GS(Th).

Since the channel is nonexistent with V₆GS = 0V and “enhanced” by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET.

Both depletion and enhancement type MOSFETs have enhancement-type regions but the label was applied to the latter since it is its only mode operation.

As V₆GS is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V₆GS constant and increase the level of V₆DS, the drain current will eventually reach a saturation level as occurred for the JFET and depletion type MOSFET. The leveling off of I₆D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel.

KVL to the terminal voltages of the MOSFET, we find that

\[ V_{DG} = V_{DS} - V_{GS} \]

If V₆GS is held fixed at some value such as 8 V and V₆DS is increased from 2 to 5 V, the voltage V₆DG will drop from −6 to −3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage V₆DG will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinched-off and a saturation condition will be established. Any further increase in V₆DS at the fixed value of V₆GS will not affect the saturation level of I₆D until breakdown conditions are encountered.
The drain characteristics shown below reveal that at $V_{GS} = 8V$, saturation occurred at a level of $V_{DS} = 6V$. In fact, the saturation level for $V_{DS}$ is related to the level of applied $V_{GS}$ by

$$V_{DSsat} = V_{DS} - V_T$$

Obviously, for a fixed value of $V_T$, then the higher the level of $V_{GS}$, the more the saturation level for $V_{DS}$ as shown by the locus of saturation levels.

As the levels of $V_{GS}$ increased from $V_T$ to 8V, the resulting saturation level for $I_D$ also increased from a level of 0 to 10 mA. It is quite noticeable that the spacing between the levels of $V_{GS}$ increased as the magnitude of $V_{GS}$ increased, resulting in ever-increments in drain current.

For values of $V_{GS}$ less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

It is the squared term that results in the nonlinear relationship between $I_D$ and $V_{GS}$. The term $k$ is a constant that is a function of the construction of the device. The value of $k$ can be determined from the following equation where $I_D(on)$ and $V_{GS(on)}$ are the values of each at a particular point on the characteristics of the device.

$$k = \frac{I_D(on)}{(V_{GS(on)} - V_T)^2}$$

Ex: substituting $I_D(on) = 10mA$ when $V_{GS(on)} = 8V$ yields

$$k = \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{(6 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2}$$

$$= 0.278 \times 10^{-3} \text{ A/V}^2$$
A general equation for $I_D$ for the characteristics shown in the previous slide results in:

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2 \text{ V})^2$$

Substituting $V_{GS} = 4\text{ V}$, we find that

$$I_D = 0.278 \times 10^{-3}(4 \text{ V} - 2 \text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$

$$I_D = 0.278 \times 10^{-3}(4) = 1.11 \text{ mA}$$

At $V_{GS} = V_T$, the squared term is 0 and $I_D = 0 \text{ mA}$.

Example (4): How to plot the transfer characteristics given the levels of $k$ and $V_T$, as included below for a particular MOSFET:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4 \text{ V})^2$$

First, a horizontal line is drawn at $I_D = 0 \text{ mA}$ from $V_{GS} = 0\text{ V}$ to $V_{GS} = 4\text{ V}$.

Next, a level of $V_{GS}$ greater than $V_T$ such as 5 V is chosen.

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4 \text{ V})^2$$

$$= 0.5 \times 10^{-3}(5 \text{ V} - 4 \text{ V})^2 = 0.5 \times 10^{-3}(1)^2$$

$$= 0.5 \text{ mA}$$

Finally, additional levels of $V_{GS}$ are chosen and the resulting levels of $I_D$ obtained.
p-Channel Enhancement-Type MOSFETs

The construction of a p-channel enhancement-type MOSFETs is exactly the reverse of n-channel type. That is, there is now an n-type substrate and p-doped regions under the drain and source connections. All the voltage polarities and the current directions are reversed. The increasing levels of current resulting from increasing negative values of $V_{GS}$.

Symbols

The symbols try to reflect the actual construction of the device. The dashed line between drain and source was chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.
Example (4): Given; $V_{GS(on)} = 10\text{V}$ will give $I_D(on) = 3\text{ mA}$. $V_{GS(TH)} = 3\text{V}$. Plot the transfer characteristics.

$\begin{align*}
E_{D} &= \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(TH)})^2} \\
E_{D} &= \frac{3\text{ mA}}{(10\text{ V} - 3\text{ V})^2} = \frac{3\times10^{-3}}{49}\text{ A/V}^2 \\
I_D &= k(V_{GS} - V_I)^2 \\
&= 0.061 \times 10^{-3}(V_{GS} - 3\text{ V})^2
\end{align*}$

For $V_{GS} = 5\text{ V}$

$I_D = 0.061 \times 10^{-3}(5\text{ V} - 3\text{ V})^2 = 0.061 \times 10^{-3}(2)^2 \\
= 0.061 \times 10^{-3}(4) = 0.244\text{ mA}$

For $V_{GS} = 8, 10, 12, \text{ and } 14\text{ V}$, $I_D$ will be 1.525, 3 (as defined), 4.94 and 7.38 mA, respectively.

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**SUMMARY**

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<tr>
<th>MOSFET</th>
</tr>
</thead>
</table>
| **depletion-type**  
| (n-channel)  
| $I_D = 0, I_R = I_S$  
| $V_D = \frac{V_{DS}}{2}$  
| $V_{DS} = \frac{V_{GS} - V_{TH}}{2}$  
|  
| MOSFET |  
| **enhancement-type**  
| (n-channel)  
| $I_D = 0, I_R = I_S$  
| $V_D = \frac{V_{DS}}{2}$  
| $I_D = k(V_{GS} - V_{TH})^2$  
| $k = \frac{V_{TP}}{V_{TH} - V_{TP}}$  

**Figure:** Graphs showing the relationship between $V_{GS}$ and $I_D$ for both depletion and enhancement-type MOSFETs. The graphs illustrate the current characteristics as a function of gate-source voltage. The resistance $R_D$ is indicated for both types, with $R_D > 10^6 \Omega$ and $C_D (1-10) \mu F$.